REMARKS

Claims 1-10, 18-19, and 22-45 are pending. Claims 1-45 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by U.S. Pat. No. 5,675,530 issued to Hirano et al. Claims 1, 18, 26-29, 32, 37, and 39 are amended. Claims 11-17 and 20-21 are canceled without prejudice.

Claim 1 is amended to recite a new use according to an embodiment of the present invention. This new use advantageously reduces noise in a memory circuit and is described in detail at page 5, lines 8-26 of the instant specification. In this embodiment illustrated by Figure 6, an active wordline couples 200 mV of noise to an adjacent and unselected wordline 106. This voltage remains on wordline 106 until the respective wordline drive circuit can restore it to 0 V. Until wordline 106 is restored to 0 V, however, subthreshold conduction of transistor 102 greatly increases. Thus, a subsequent low-high-low pulse of a plateline PL 110 imparts a small negative voltage to storage node 112. This negative voltage or noise accumulates with each subsequent activation of the adjacent wordline and may result in read errors or even depolarization of the ferroelectric capacitor.

Claim 1, as amended, recites "*A method of reducing noise voltage in a memory circuit*, comprising the steps of: *activating a first signal line adjacent a control terminal of a memory cell; coupling a voltage from the signal line to the control terminal of the memory cell; applying a second control signal to the memory cell; coupling the noise voltage to the memory cell in response to the step of applying the second control signal*; activating a precharge signal applied to a precharge circuit to precharge a bitline connected to the memory cell to a predetermined voltage; activating a first control signal from an inactive state after the step of coupling while the precharge signal is active, the first control signal applied to the control terminal of the memory cell, the memory cell having a current path connected to the bitline, wherein the noise voltage is conducted to the bitline through the current path; and inactivating the precharge signal while the first control signal is active." (emphasis added).

Referring back to Figure 6, the new use of the present invention to reduce noise voltage in a memory circuit first includes the new step of "activating a first signal line adjacent a control terminal of a memory cell." This is a wordline adjacent to wordline 106 as described at page 4, line 30 through page 5, line 1. The second new step includes "coupling a voltage from the signal line to the control terminal of the memory cell." This is described at page 5, lines 1-2. The third new step is "applying a second control signal to the memory cell." This is the plateline signal applied to lead 110 as described at page 5, lines 2-3. Finally, the step of "coupling the noise voltage to the memory cell in response to the step of applying the second control signal" is described at page 5, lines 13-26. The present new use invention removes most of the noise voltage imparted to storage node 112 by "activating a first control signal from an inactive state while the precharge signal is active" as recited by claim 1. These steps are not disclosed by Hirano et al. By way of contrast, the disclosure of Hirano et al. is limited to reducing an electric field which remains in the capacitor after a memory cell is accessed. (col. 1, line 60-col. 2, line 16). Thus, applicant believes claim 1, as amended, and depending claims 2-10 are patentable under 35 U.S.C. § 102(b).

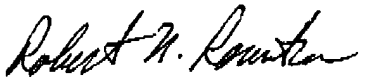
Amended claim 39 also recites the new use as previously described with respect to claim 1. Claim 39, as amended, recites "*A method of operating a memory circuit to reduce a charge coupled to a memory cell*, comprising the steps of: *coupling the charge to the memory cell while a first control signal applied to a control terminal of the memory signal is inactive*; activating a precharge signal applied to a precharge circuit to precharge a bitline to a predetermined voltage; activating the first control signal while the precharge signal is active, the first control signal applied to the control terminal of a memory cell of the memory cell, the memory cell having a current path connected to the bitline; *conducting at least a part of the charge to the predetermined voltage*; applying an inactive second control signal to the memory cell; then inactivating the precharge signal; and then activating the second control signal." (emphasis added). Claim 39 recites a method to reduce charge coupled to a memory cell. In particular, this charge is coupled to the memory cell while a first control signal applied to a control terminal is inactive. Referring back to the embodiment of Figure 6 of the instant specification, this charge is coupled to the memory cell while the signal at wordline

106 is inactive. This step is not disclosed, taught, or suggested by Hirano et al. Thus, applicant respectfully submits that claim 39, as amended, and depending claims 40-45 are patentable under 35 U.S.C. § 102(b).

Claims 18, 26, and 32 and their respective depending claims are rejected under 35 U.S.C. § 102(b) as being anticipated by Hirano et al. Claim 18 is amended to recite "a plateline circuit arranged to *apply a first plateline signal pulse* to the respective row of memory cells *to produce a difference voltage* between the bitline and the complementary bitline and to *apply a second plateline signal pulse to restore data to the respective row of memory cells*; and a sense amplifier circuit arranged to amplify the difference voltage." Claim 26, as amended, recites "a plateline circuit arranged to *apply a first plateline signal pulse* to a memory cell including the first and second access transistors *to produce a difference voltage* between the bitline and the complementary bitline and to *apply a second plateline signal pulse to restore data to the memory cell*; and a sense amplifier circuit arranged to amplify the difference voltage." Claim 32, as amended, recites "a plateline circuit arranged to *apply a first plateline signal pulse* to a memory cell including the access transistor *to produce a difference voltage* between the bitline and the complementary bitline and to *apply a second plateline signal pulse to restore data to the memory cell*; and a sense amplifier circuit arranged to amplify the difference voltage." (emphasis added). This embodiment of the present invention is shown at Figures 7 and 8B and described in detail at page 10, line 18 through page 11, line 23. Hirano et al. fail to disclose these features of the present invention. Thus, applicant respectfully submits that claims 26-28 and 30-38 are patentable under 35 U.S.C. § 102(b).

In view of the foregoing, applicants respectfully request reconsideration and allowance of claims 1-10, 18-19, and 22-45. If the Examiner finds any issue that is unresolved, please call applicant's attorney by dialing the telephone number printed below.

Respectfully submitted,



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